Indian Institute of Technology Kharagpur
Department of Computer Science & Engineering
Spring Semester 2006

Course : **CS 60046 Low Power Circuits & Systems**
Credits : 3-0-0
Faculty : Ajit Pal
Lecture hours : **WED-5, THU-4, FRI-2-3** Room #: **108**, CSE Building
TA of the course : Prashant Agrawal

Scope: In recent years, power dissipation has emerged as the key issue not only for portable computers and mobile communication devices, but also for high-end systems. Reducing power dissipation is of primary importance in achieving longer battery life in portable devices. On the other hand, for high-end systems the cooling and packaging requirements are pushing the chip designers for low power alternatives. As a consequence, apart from the size, cost and performance, now-a-days power is considered as the most important constraint. The objective of this course is to provide a comprehensive coverage of different aspects of low power circuit synthesis at various levels of design hierarchy.

Prerequisite: The students should have good background on digital circuits (should have attended a course on digital circuits). No background in the area of VLSI circuits is required.

Text/Reference Books:

T1 Sung_Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgrag Hill

T2 Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint).

T3 A. Bellamour, and M. I. Elmasri, *Low Power VLSI CMOS Circuit Design*, Kluwer Academic Press, 1995

T3 Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995

R1 Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Interscience, 2000

Evaluation:

Mid-term	30%
End-term	50%
Term Assessment	20%

Course Outline:

1. Basics of MOS circuits:
   - MOS Transistor structure and device modeling
   - MOS Inverters
   - MOS Combinational Circuits – Different Logic Families
2. Sources of Power dissipation:
   - Static Power Dissipation
     i. Diode Leakage Power
     ii. Subthreshold Leakage Power
     iii. Leakage power DSM circuits
   - Dynamic Power Dissipation
     i. Short Circuit Power
     ii. Switching Power
     iii. Gliching Power
   - Degrees of Freedom
3. Supply Voltage Scaling Approaches:
   - Technology Level – Feature Size Scaling, Threshold Voltage Reduction
   - Logic Level – Transistor sizing, Multiple Vt Circuits, Logic styles for Low Power, Synthesis of Low Power CMOS Circuits
   - Architecture Level – Parallelism and Pipelining
   - Algorithm Level – Transformations to exploit Concurrency
4. Switched Capacitance Minimization Approaches:
   - System Level – Power Down, System Partitioning
   - Algorithm Level – Concurrency, Locality, Regularity, Data Representation
   - Architecture Level – Concurrency, Signal Correlation
   - Logic Level – Transistor sizing, Logic Optimization
   - Layout Level – Layout Optimization
   - Technology Level – Advanced Packaging, SOI
5. Special Topics:
   - Adiabatic Switching
   - Battery-aware Synthesis